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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,663	10/07/2003	Wenbin Jiang	4161-PA1C	7292

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EXAMINER	
SINGH, DALZID E	

ART UNIT	PAPER NUMBER
2633	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,663	JIANG ET AL.	
	Examiner	Art Unit	
	Dalzid Singh	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because the structural elements of figure 1 (110, 112, 114, 116, 118, 120 and 150) and figure 2 (210, 212, 214, 216, 218, 220, 250 and 252) are merely labeled with identifying numbers. Applicant must supply a suitable legend. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application (see 37 CFR 1.84(n) and 1.84(o)). The objection to the drawings will not be held in abeyance.

The following are direct quotations of 37 CFR 1.84(n) and 1.84(o), repeated below:

> (n) *Symbols*. Graphical drawing symbols may be used for conventional elements when appropriate. The elements for which such symbols and labeled representations are used must be adequately identified in the specification. Known devices should be illustrated by symbols which have a universally recognized conventional meaning and are generally accepted in the art. **Other symbols which are not universally recognized may be used, subject to approval by the Office, if they are not likely to be confused with existing conventional symbols, and if they are readily identifiable.**
>
> (o) *Legends*. **Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing.** They should contain as few words as possible.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the data management circuitry, cited in claims 14 and 22, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 23-29 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2, 4 and 7-9 of U.S. Patent No. 6,665,498. Although the conflicting claims are not identical, they are not patentably distinct from each other because the current application and the patent both claimed the same subject matter.

Regarding claim 23, the patent claims a high-speed optical data link (see claims 1 and 2) comprising:

a system circuit board;

a first ASIC mounted on the system circuit board;

a second ASIC mounted on the system circuit board;

optical receiver having an amplifier (since the claim indicates one of receiver and transmitter, therefore a receiver is selected); and,

board level IC coupled to the ASIC (see claim 2).

The patent differs from the current application in that the patent does not specifically disclose that the board level IC is coupled to the second ASIC. However, as indicated in claim 2 of the patent, the second ASIC is coupled to the board level IC. In claim 1, the patent indicated that the second and first ASIC are electrically coupled. Therefore, it would have been obvious that the second ASIC is coupled to the board level IC through the first ASIC. Furthermore, claim 5, discloses a first ASIC coupled to the board level IC.

Regarding claim 24, as indicated in claim 1, the patent discloses that the first ASIC and second ASIC are electrically coupled and differ from the claimed invention in that the patent does not disclose carrying electrical signal at a rate equal to at least 5-gigabits per second. However, in claim 8, the patent discloses that the rate is at least 10 gigabits per second. Therefore, it would have been obvious to an artisan of rodinary skill in the art to modify the interface as disclosed by the patent to operate at 5 gigabits

per second. One of rodinary skill in the art would have been motivated to do this in order to provide compatibility between various other interfacing devices.

Regarding claim 25, as indicated in claims 1, 4 and 7, the patent discloses that the first and second ASIC includes clocking and equalization/retiming function for sending and recovering data.

Regarding claim 26, as indicated in claim 1, the patent discloses that the amplifier of the receiver includes photodiode and a trans-impedance/post-amplifier.

Regarding claim 27, the patent discloses a high-speed optical data link, as discussed in claim 7, comprising:

a system circuit board;

a board level IC (see claim 5), which is coupled to an ASIC;

a fiber optical receiver; and,

a fiber optical transmitter.

The patent differs from the claimed invention in that the patent does not disclose carrying electrical signal at a rate equal to at least 5-gigabits per second. However, in claim 8, the patent discloses that the rate is at least 10 gigabits per second. Therefore, it would have been obvious to an artisan of rodinary skill in the art to modify the interface as disclosed by the patent to operate at 5 gigabits per second. One of rodinary skill in the art would have been motivated to do this in order to provide compatibility between various other interfacing devices.

Regarding claim 28, in claim 8, the patent discloses:

providing system circuit board;

receiving electrical signal;

clocking and equalizing/retiming the electrical signal;

conveying the equalized signals to a second position; and

receiving and recovering the signal.

The patent differs from the claim in that the patent does not disclose first position. However it would have been obvious to indicate different position of the circuit board as first or second position. Furthermore, the patent differs from the claimed invention in that the patent does not disclose carrying electrical signal at a rate equal to at least 5-gigabits per second. However, in claim 8, the patent discloses that the rate is at least 10 gigabits per second. Therefore, it would have been obvious to an artisan of rodinary skill in the art to modify the interface as disclosed by the patent to operate at 5 gigabits per second. One of rodinary skill in the art would have been motivated to do this in order to provide compatibility between various other interfacing devices.

Regarding claim 29, as indicated above and in claims 1, 4 and 7 of the patent, the signal is recovered through the use of clocking and equalization/retiming step.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dalzid Singh whose telephone number is (571) 272-3029. The examiner can normally be reached on Mon-Fri 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571) 272--3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DS
October 21, 2004
David Singh